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Experimental Analysis and Investigation on the Effects of Radiations on Integrated Circuits for Space Applications

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Abstract: **In this article the effects of radiations on discrete and complex electronic devices were analyzed. In the preliminary phase of this work the space environment was studied, referring to radiations and their effects on the matter and on electronic devices. The main radiation-hardening techniques were investigated, in particular the "by-layout" techniques. One of these rad-hard devices is the edgeless transistor (ELT). A static electrical characterization, before the irradiation (fresh condition), was conducted on these devices in order to evaluate their features with respect to the standard ones (STD). The measures have highlighted the differences between the ELT types, confirming the main features of ELTs, as shown in literature as well. Another investigation regarded the irradiation test of some 8Mbit TOPAZ flash memories using Boron ions. These test were conducted both in the active state (during the reading of memory cells) and in the passive state (in standby). Thanks to these test, it was possible to study the memory cell bit flips at the changing of the radiation dose, classifying the different bit flip stories dose by dose. Finally, the result was that: the flips of programmed bits were more frequent than ones of non-programmed bits; the memories irradiated in active state had less failures than the ones irradiated in passive state. Some statistical data elaborations were conducted in order to understand the trend of the bit-flip of the cells with the dose. Using these data a predictive model was defined to estimate the mean variation of the memory cell threshold voltage shift with the dose.**

Keywords: **Radiations, Total dose, ELT transistors, pre/post irradiation measurements.**

I. INTRODUCTION

Nowadays, in the space field there is more and more the need to have devices which could work properly under harsh conditions of radiation [1], [2], without suffering severe damages [3], [4]. Often, high radiation-hardness capabilities corresponds to very high cost, because of the use of non-standard technology. The alternative choice could be the use of some design tricks and layout to obtain good level of radiation-hardness, using standard CMOS technology processes [5]. There are several different techniques which allow to increase the radiation-hardness of a system [6]. These techniques can be based on the use of commercial parts in redundant and duplicative configurations (radiation hardening by architecture) [7], the employment of specific material and processing procedure (radiation hardening by process) [8], the design of dopant wells and isolation trenches into the chip layout (radiation hardening by layout) [9]. Considering the specific final application, it is possible to select one of these techniques to develop a radiation-tolerant system, because each technique has pros and cons. It is important also to distinguish between Total Dose Effects (TDE) and Single Event Effects (SEE) [10], [11] on the electronic devices. The first effects are due to the cumulative damage of the semiconductor lattice caused by ionizing radiation over the exposition time and they could affect both analog and digital devices; the latter affect mainly the digital devices and are due to high-energy a particle which travels through the semiconductor

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leaving an ionized track behind. This ionization may cause different effects, depending by several parameters (particle energy, angle, linear energy transfer, flux, atomic mass, etc), such as a benign glitch in output, a less benign bit flip in memory or a register, especially, a destructive latch-up and burnout in high-power transistors. In this work the TDE were studied and treated [12], [13].

II. SPACE RADIATION ENVIRONMENT AND EFFECTS ON MOSFET DEVICES

The radiation aspect of the space environment is almost always the main problem to face into the design and realization of electronic devices for space applications.

In the space there are a lot of different radiations: solar radiations, cosmic rays, deep space radiations, etc., and many phenomena connected to them, such as solar and universal magnetic storms which can cause several serious damages and troubles to the instruments. The particle which interacts with the devices is divided into two categories: charged (electrons, protons, heavy ions) and neutral (photons, neutrons), they can cause two damage phenomena: the ionization and the nuclear dislocation (Frenkel) respectively.

To define the dose entity the *Rad* is used as measure unit, it is 0.01 J/kg. To compare two different radiation types the LET (Linear Energy Transfer) is used, it is measured in [$MeV*cm^2*mg^{-1}$] and shows the ionizing capability of a radiation and the energy released to the matter [14].

$$LET = \frac{1}{\rho}\frac{dE}{dx} \qquad (1)$$

It increases with the particle mass and charge and decreases with its velocity. Hence, the heavy ions, protons and □□particles have an high LET while □□rays, X rays, □□particles and electrons have a low LET. The radiations with low LET have a spread and low density ionizing effect into the matter while the ones with high LET creates more focused and high density ionizations [15].

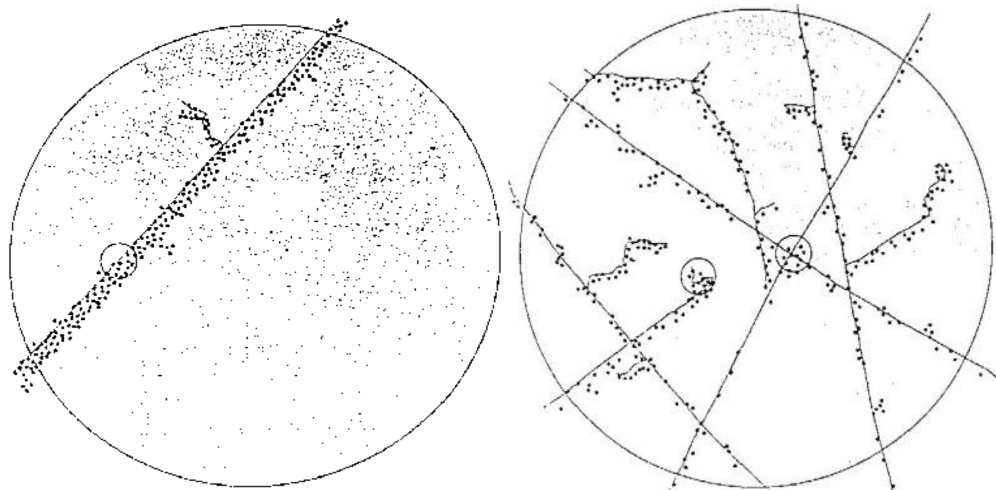

Fig: 1 High and Low LET effect

In MOS circuits, the more radiation sensitive part is the oxide [16]. The main phenomenon is the ionization, which leads to the electron-hole pair generation; after the irradiation part of e/h pairs recombine and disappear, the number of recombination depends on the LET value of the incident radiation and on the electrical field *E* applied; it scales directly with the radiation LET and inversely with *E*. The e/h pairs which remain, because of the highest mobility of electrons, leave spurious holes which can generate:

- Fixed charge into the oxide;
- Trapped charge at the interface S_iO_2/S_i.

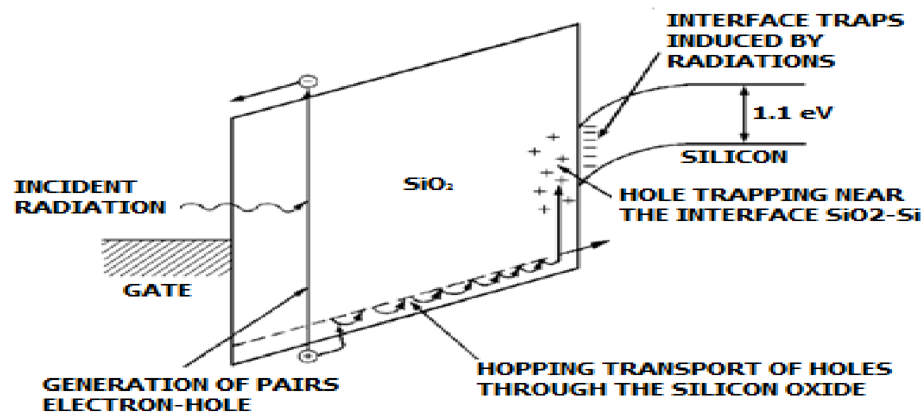

Fig.2 Radiation effect in a MOS circuit.

In the case of nMOS, the fixed charge will be very near to the interface causing important effects [17], while in the case of pMOS, the holes will be trapped deeply into the oxide with minor effects [18].

After the irradiation there is an increasing of the number of interface traps which will be filled with electrons (nMOS case) or holes (pMOS case) but their effect will become important later than the effect of fixed charges. It is also possible that the trapped holes are neutralized by the tunnel effect of electrons from the channel (thanks also to the *E* field which increases the effect) or by thermic effects which puts electrons from the oxide valence band to the conduction band.

These trapped charges lead to the following effects [19], [20], [21]:

- *Threshold voltage shift:*

$$\Delta V_T = \Delta V_{ox} + \Delta V_{it} = -\frac{Q_{it}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \qquad (2)$$

with the two contributions due to fixed charges into the oxide and the trapped charges at the interface, respectively.

ΔV_{ox} is negative for the nMOS and positive for the pMOS; ΔV_{it} is positive for both the devices.

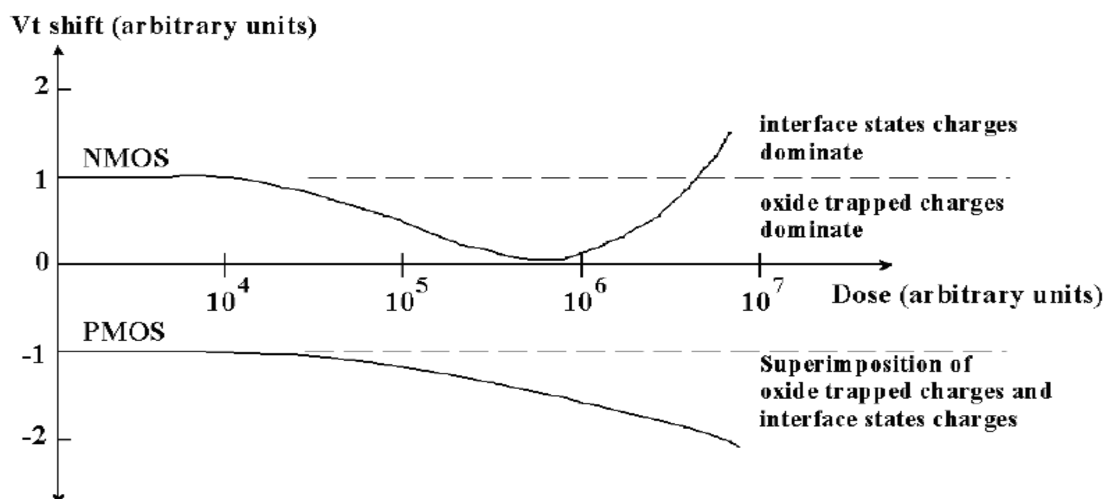

Fig.3 Vt profile on varying of dose.

The Vt trend on varying of dose is explained considering the absolute value of ΔV_{ox} decreases with the dose while the one of ΔV_{it} increases (maintaining both the same sign) because of the increasing of charges into the traps. This condition makes the pMOS radiation-hard with respect of nMOS.

- *Sub-threshold slope variation:*

$$\Delta S = \frac{kT}{q} \cdot \ln 10 \cdot \frac{q \Delta D_{it}}{C_{ox}} \qquad (3)$$

It is due to the increasing of traps density and so to the threshold voltage variation; it regards only the nMOS.

- *Increasing of sub-threshold and leakage currents:*

The sub-threshold currents are caused by the decreasing of threshold voltage and of sub-threshold slope. The leakage currents are caused by the field oxides which separate the devices and storing holes create parasitic paths between drain and source (Fig.4), modifying the electrical features of MOSFET.

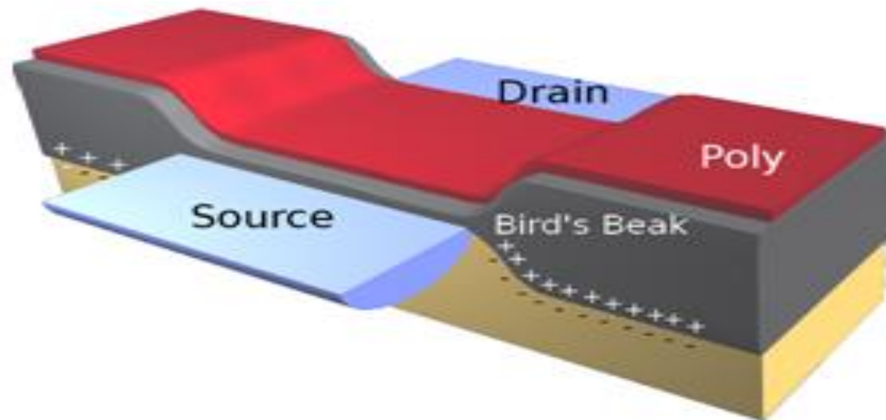

Fig.4 Bird's beak effect

- *Decreasing of trans-conductance g_m and mobility* □□

Because of the interface traps there is a decreasing of mobility and so of trans-conductance.

These problems can be minimized using several radiation-hardness techniques.

III. ELT TRANSISTORS

As already said, there are several rad-hard approaches in literature. In this work the technological approach was studied [22], [23], [24], [25]. In particular, the edgeless transistors (ELT) were investigated [5]. These devices allow to solve the problem of the leakage currents inside the *bird's beaks*.

They have a typical ring-like structure. The drain can be inside the ring and the source outside or vice versa (Fig.5). In this way without oxides between the drain and source regions there are not parasitic paths anymore and so the leakage currents disappear.

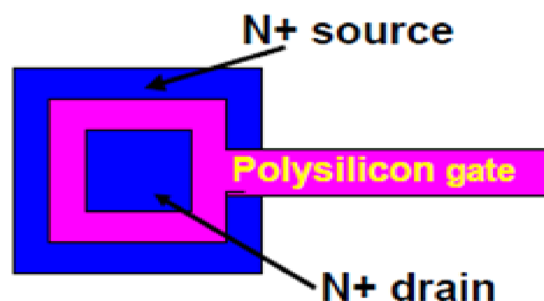

Fig.5 ELT structure

This structure has some problems:

- The aspect ratio W/L in not well-defined;
- The used area is high;

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- There are electrical parameter asymmetries due to the different configurations (drain-out, drain-in).

In the literature many differences between the drain-out and drain-in cases are underlined :

- $G_{d,in} > G_{d,out}$ $G_{m,in} > G_{m,out}$
- $I_{d,in} > I_{d,out}$ $C_{gd,in} < C_{gd,out}$

Where G_d is the output conductance, G_m is the trans-conductance, C_{gd} is the gate-drain capacity and I_d is the drain current.

These differences are mainly due to an higher electrical field concentrated inside the ring which leads to have higher levels of current and output conductance.

IV. ELECTRICAL CHARACTERIZATION OF ELTs

In order to verify what is in literature, several static electrical measurements (Vds-Id and Vgs-Id) were conducted on ELT nMOS transistors and STD (standard) nMOS transistors of two types: 1.8V (Fig.7) and 3.3V.

The 1.8V ELT transistors are designed with three different gate contact types: one, two and four gate sides contacted (Fig.6). This test was done to evaluate the electrical differences among these transistors and to establish the advantage to choose one of them. This point is important for the ELT technology because more contacts are designed more area is used to build the MOSFET inverter. The 3.3V ELT transistors are designed all with four gate sides contacted. All the ELT transistors are designed with an aspect ratio W/L of about 12.99 in order to be as similar as possible to the aspect ratio of STD transistors (about 12.65). This W/L of the ELT transistors is an effective value provided by the CADENCE design software tool. These transistors were designed by RedCat Devices company using a 0.2um (t_{ox}=4nm) CMOS technology for the 1.8V version and a 0.4um (t_{ox}=6.4nm) CMOS technology for the 3.3V version.

At the end of these measurements the results were:

- Although the company which provided the devices designed the ELT transistors with an aspect ratio W/L similar to that one of the STD transistors, there are some differences, for example: I_d current. This condition would demonstrate that, even if the two transistors have a W/L similar, their different structure gives different results. Hence, it would need to define a proper correction factor during the device design phase;
- The three types of ELT (1.8V) with one, two and four gate sides contacted have just little differences both of I_d current and of the electrical parameters G_d and G_m, so it is possible to save area using the type with one gate side connected (Fig.8);
- It is confirmed, for all the ELT transistor types, what the literature [5] says concerning the differences of the electrical parameters G_d and G_m in the two cases drain-in and drain-out; confirming also that if $L < 0.5$ um (in our case L = 0.2 um) the value of output conductance $G_{d,in}$ of a STD transistor is about the value of $G_{d,in}$ of a ELT transistor (Fig.9);
- The STD transistors have the I_d current and the electrical parameters G_d and G_m higher than those ones of the ELT transistors.

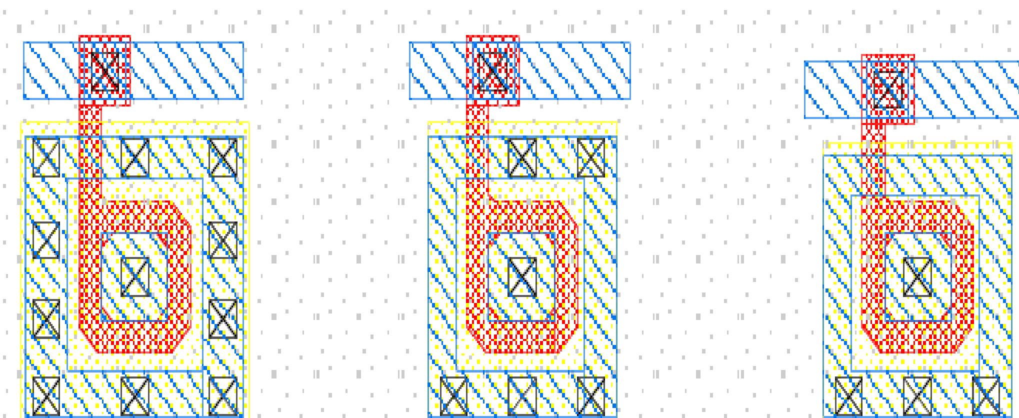

Fig.6 1.8V ELT transistors with one, two and four gate sides contacted

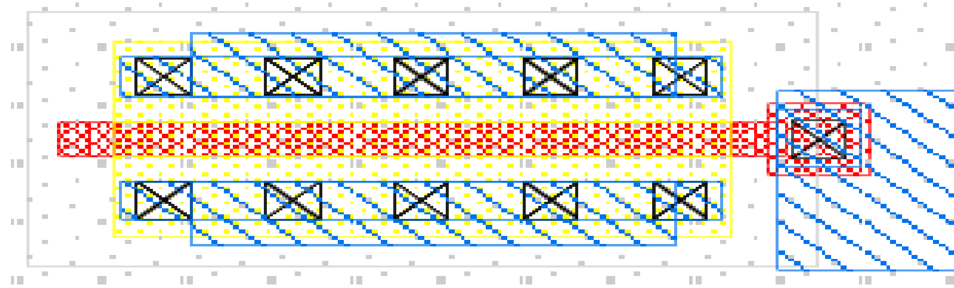

Fig.7 1.8V STD transistor

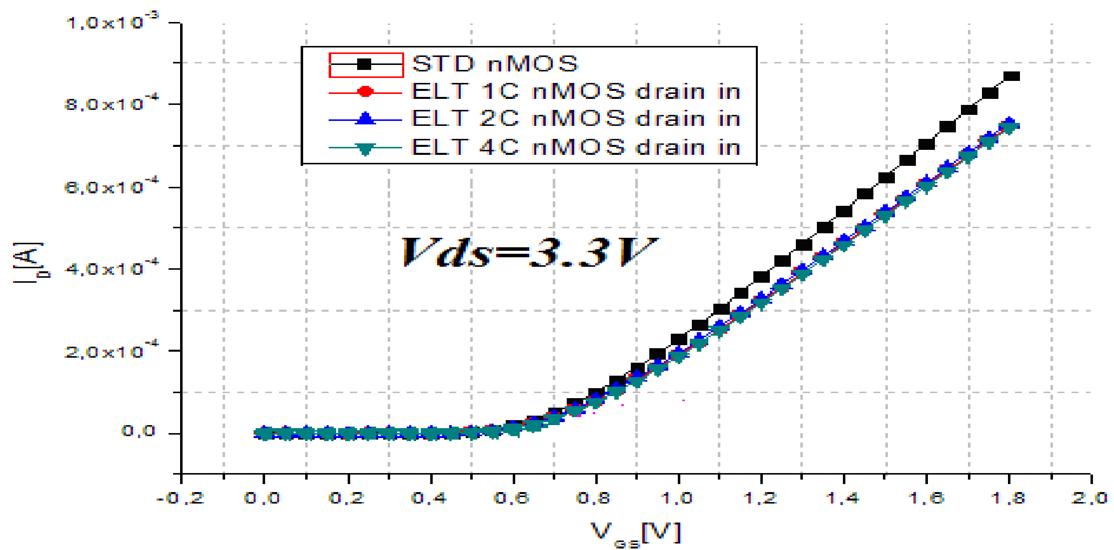

Fig.8 I_d-V_{gs} in saturation

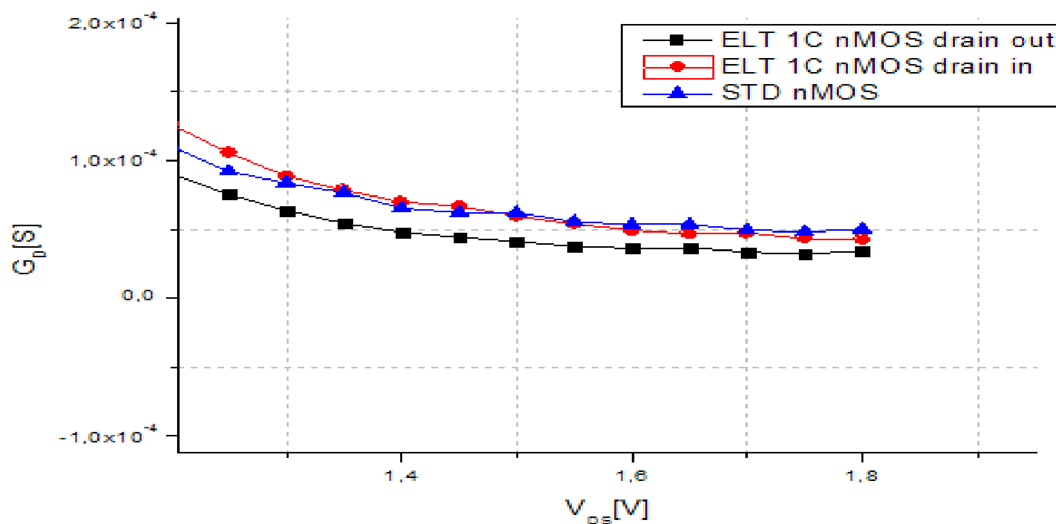

Fig.9 Output conductance trend G_d-V_{ds}

V. RHESSA BOARD AND TOPAZ MEMORY

Another aspect investigated in this work was the radiation hardness, in particular the Total Dose hardness, of a TOPAZ flash memory [26]. The proper working of this memory had to be tested under radiation with the aim of defining its level of radiation-tolerance. In order to conduct the test under radiation, a testing board was used. This board was developed by Technosystem Development company, within the RHESSA project [27]. This board allows both to provide power to the

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memories during the *active* test (reading mode test) and to store, onto a proper SRAM memory, the fault locations of the flash memory for the post-processing phase.

The boards (Fig.10) is based on an FPGA (ProASIC Actel) which manages and control all the memory operations (programming, reading, deleting, etc) and allows the user to interact with the board by remote, using a GUI software. It can control two TOPAZ flash memories mutually, guaranteeing a cold redundancy of working.

It is 5V powered and using some regulation circuits three voltage reference: 1.8V, 2.5V and 3.3V are obtained. The 1.8V and 3.3V voltages are necessary to power the TOPAZ memories while the 2.5V is used for other supporting circuits. There is also an anti-latch-up protection circuit which monitors the power supply currents of TOPAZ memories and allows to turn the power down as fast as possible when an over-currents. The protection works when the current value is higher than a threshold, settable by the user.

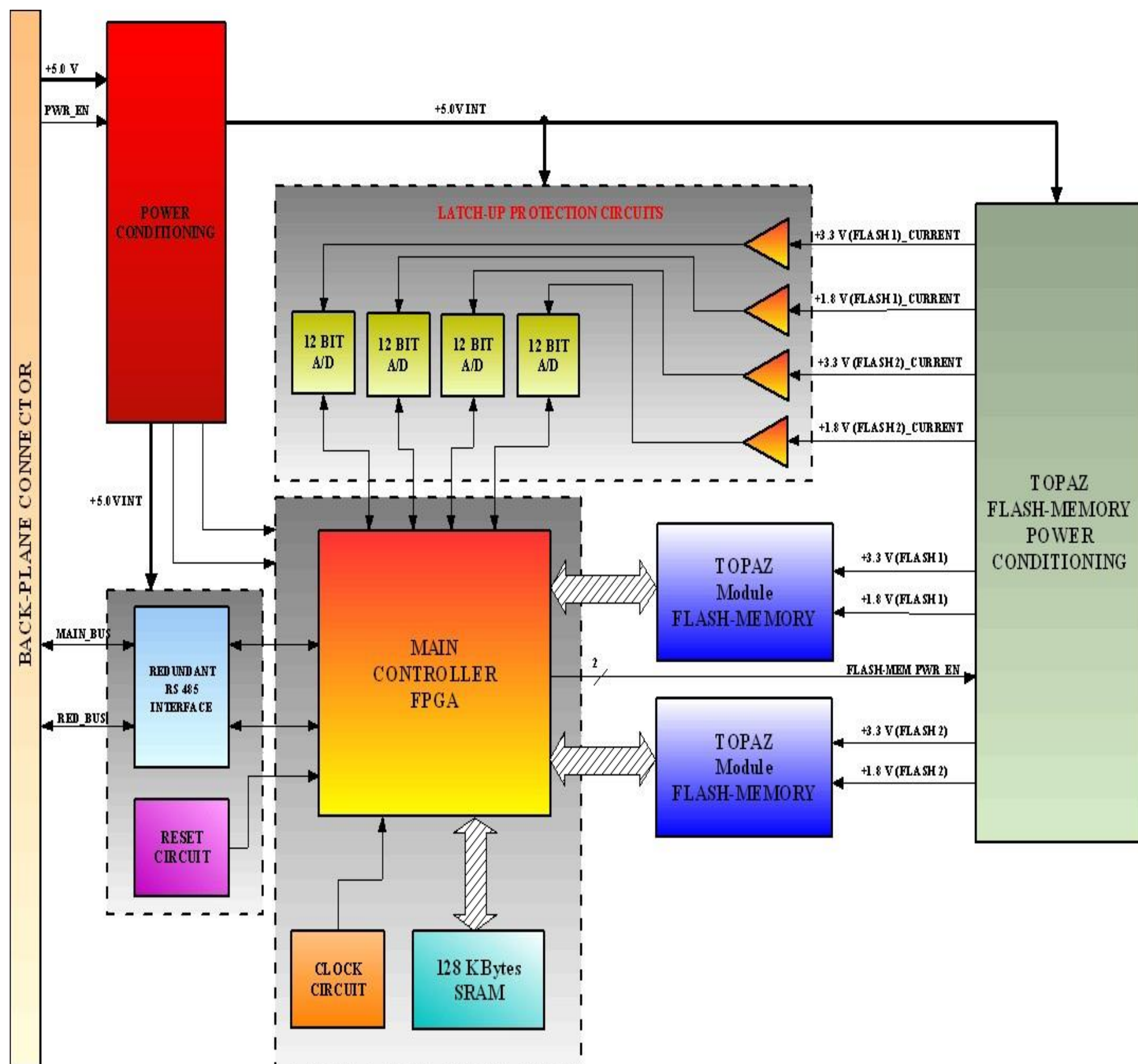

Fig.10 RHESSA board block diagram

Because of the effects of radiation on the electronic devices, it could be possible to cause the fault of the memory. The main effect is the increasing of the device current absorption up to the latch-up, that is a circuit-short between VCC and GND. For this motive, the efficiency of this protection circuit was evaluated conducting some test using different resistors (18, 47, 68, 330 ohm) connected between the terminals (VCC and GND) of the power supplier (1.8V and 3.3V) in order to change the load current. For each different load current, a proper current threshold is set to induce the protection intervention. Fig.11 shows the measurement setup.

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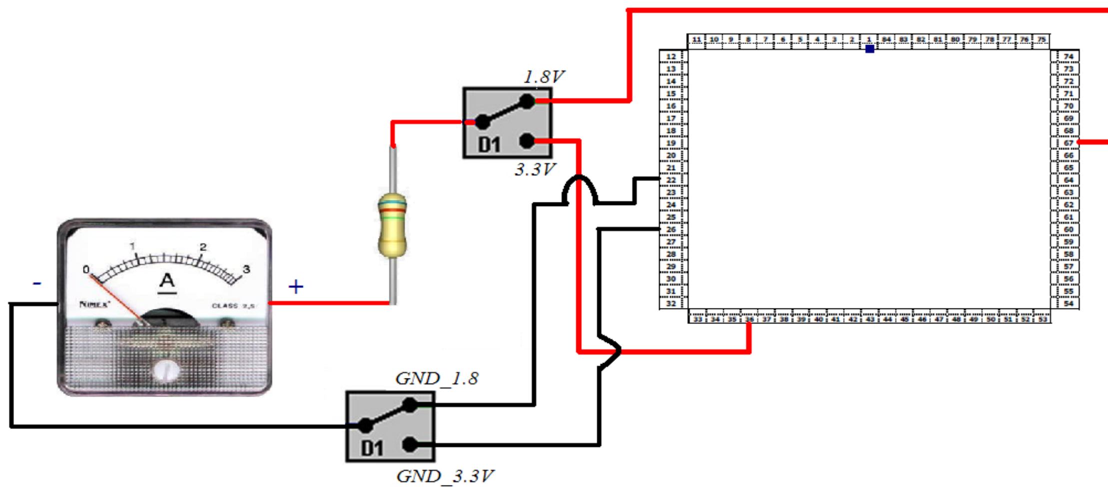

Fig.11 Test setup for the latch-up protection circuit

Thanks to this test, a system bug was found. For example, using the 47 ohm resistor on the 3.3V power line, a 68.71 mA current was absorbed and although the current threshold was set to 50mA the protection did not go off. There problem was in the calibration system because the real value, which was evaluated by the system , was not 68.74 mA but about 33.023 mA (half of the actual value) so lower than 50 mA (current threshold set). For this motive the protection was not activated. By the way, without considering the bug, the good state and accuracy of the protection system was verified.

The TOPAZ flash memory is formed by 8M cells NROM and its size (W*L = 0.42 um * 0.18 um) is 0.0756 um^2. It is divided into 19 sectors (but just 15 sectors with 32K words) which can be programmed, red and deleted independently. As already said, it needs two power references (1.8V and 3.3V) for reading and programming/deleting operations respectively. In reality, the physical programming/deleting of the cells is possible applying a higher voltage level, obtained using a step-up converter to increase the voltage from 3.3V to about 10V. This memory absorbs about 800 nA and 700 uA during the Stop and Standby phase respectively and 19 mA and 14-15 mA during the reading and programming/deleting respectively. The reading time is about 49 ns and the programming time for a word is about 35.6 us. The block diagram of the memory is shown in Fig.12.

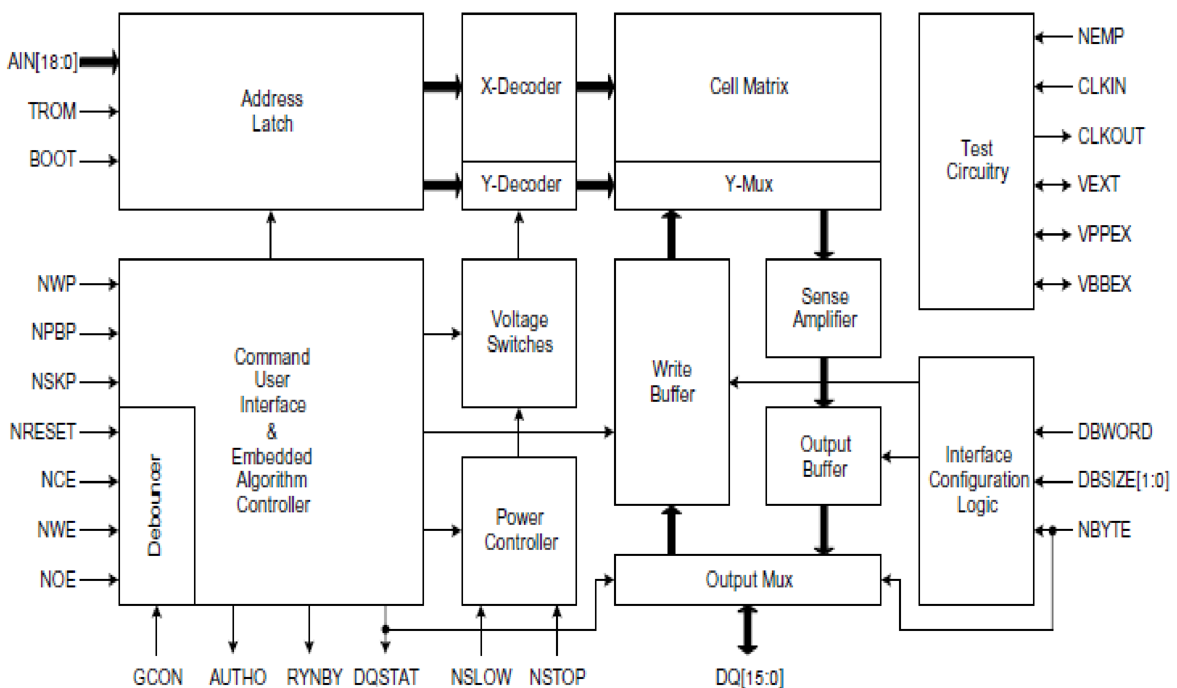

Fig.12 TOPAZ memory block diagram

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VI. TOPAZ MEMORY IRRADIATION TEST

Usually, in order to test the Total Dose hardness of an electronic device, X rays or gamma rays are used, but in our case the irradiation test were conducted using 10 MeV Boron ions, at the CNR (National Research Council) of Catania (Italy). These ions have not a a high atomic mass, and so they are not considered real heavy ions. For this motive they could be used for TD test as well.

Two different TOPAZ memory chips were irradiated [27], [28]; one (205) was irradiated in *active* state and the other one (220) in *passive* state. All the sectors were pre-programmed with fixed data patterns, as shown in Table I. It needs to say that a "1" logic value corresponds to a no-programmed cell and a "0" logic value to a programmed cell.

TABLE I: DATA PATTERNS PRE-PROGRAMMED INTO THE MEMORY SECTORS

PATTERN	*0000*	*AAAA*	*5555*	*FFFF*
SECTORS	*SA4*	*SA5*	*SA6*	*SA7*
	SA8	*SA9*	*SA10*	*SA11*
	SA12	*SA13*	*SA14*	*SA15*
	SA16			
	SA17			

The ions fluences used during the irradiation test were between 10^9 and $2.5*10^{10}$ ions/cm^2 corresponding to the dose levels of 56 krad and 1.4 Mrad. After each cumulative dose of irradiation the number of faults (bit-flip) of the cells of each sector. For each dose, an average of the number of faults inside the sectors with the same data pattern stored was calculated. Some graphs are plotted to show the trend of the mean number of faults at the changing of the dose and of the data pattern, both for the *active* state and the *passive* state. These graphs are shown in Fig.14.

It is possible to see that the fault percentage in the *passive* case (T220) is pretty higher than that one in the *active* case (T205), concerning the sectors with "0000", "AAAA" and "5555" data patterns. As regards the sectors with "FFFF" data pattern, the situation is different: the faults are evident at a very high dose level (>$7*10^9$ ioni/cm2); the fault percentage in the *active* case higher than that one in the *passive* case, with an higher trend slope as well.

Generalizing these results, at low doses levels, the programmed cells have higher probability to have bit-flips than those ones no-programmed. At high dose levels the situation is the opposite.

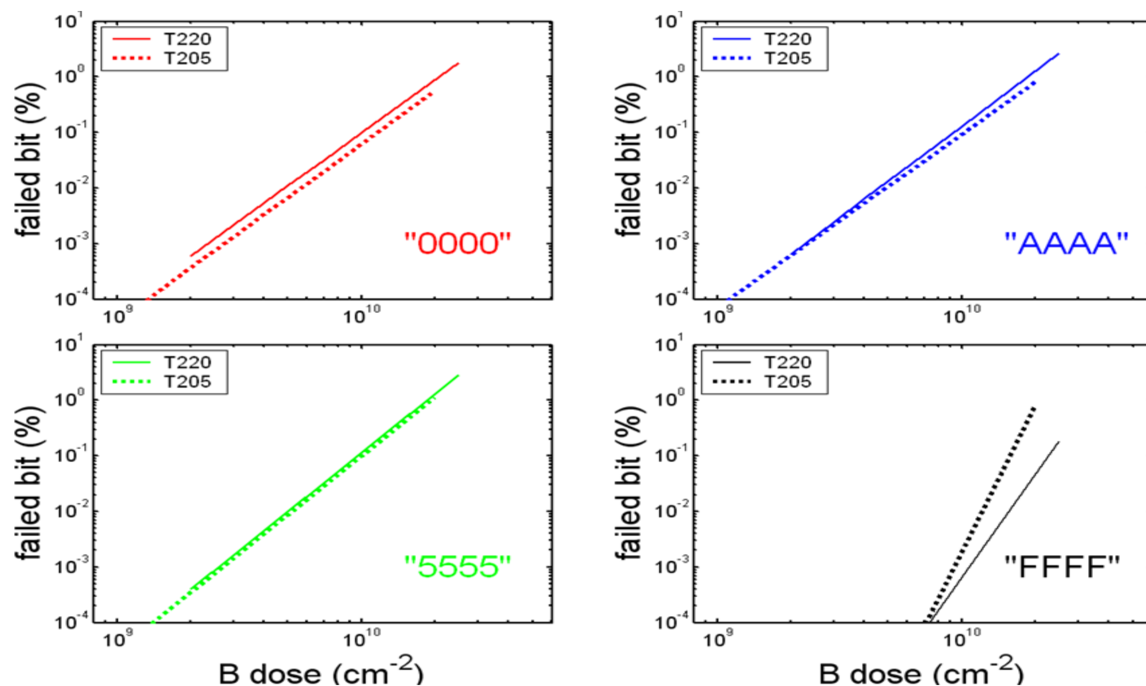

Fig.13 Trend of the failed bit changing the dose level, for the four data patterns (0000, AAAA, 5555, FFFF) and the two working modes: *active (T205)* and *passive (T220)*

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The difference between the *active* and *passive* case, at low doses, could be explained considering the presence of the electrical field which eases the electron tunneling from the channel to the oxide and the recombination with the holes induced by the radiation. The difference between the behavior of the programmed and no-programmed cells, at low doses, is, obviously, because the threshold voltage of the cells, on average, tends to decrease, so it will be easier that a bit "0" becomes "1" than the opposite. At high doses, the threshold voltage begins to have a positive shift and so the probability of a "1" to "0" bit-flip increases. It is necessary to mind, from the literature, that the threshold voltage shift probability distribution for a memory has a Gaussian shape curve with its peak for negative voltage shifts and its tails for positive values. This curve, increasing the dose, shifts up to having its peak also for positive V_t voltage shifts.

With the aim to analyze the behavior of the cells during the time, the data of the memories were analyzed after some months from the irradiation test. The results were that the mean number of faults (bit-flips) in the memories is increased. This situation can be justified both taking into account the interface traps increasing with the time, as explained in literature and the failure of the on-memory control electronics after high radiation dose levels (1.4 Mrad). The failure of the control electronics surely happened after the 1.4 Mrad dose level, in fact, after deleting some sectors, it was not possible to programming or reading again these sectors. These last considerations can be understood considering that the high voltage (about 10 V), necessary for programming/deleting the cells, can have compromised these circuits in an irreversible way.

Considering that up to 396krad ($7*10^9$ ions/cm^2) all the sectors worked well, the data analysis was conducted elaborating the data up to this dose level.

After a year from the irradiation test, five consecutive reading of the sector #5 of the memory 205 (*active* case) were done. This sector was used for the test, in order to have an average between the behavior of a programmed and no-programmed cell (being programmed with a "AAAA" pattern, it has the same number of "0" and "1" bits). Fig.14 shows that after the first reading, most bits maintains their logic state, while a little part of bits change their state. This second behavior can be due to the presence of the electrical field which can ease the electron injection inside the nitride, forcing the programming of these cells; then, these electrons could recombine with the trapped holes, disappearing. So these events could provoke the variable reading. The x-axis of the graph in Fig.14 represents the bit-flip reading distribution (from the first to the fifth reading) of the cells; each bit-flip reading type shows five logic values of a cell, corresponding to each single reading (i.e.: **00001** => $\mathbf{0}_{1}{}^{st}{}_{read.}$- $\mathbf{0}_{2}{}^{nd}{}_{read.}$- $\mathbf{0}_{3}{}^{rd}{}_{read.}$- $\mathbf{0}_{4}{}^{th}{}_{read.}$- $\mathbf{1}_{5}{}^{th}{}_{read.}$). The y-axis is the number of cell of the sector #5 which follow a given reading evolution.

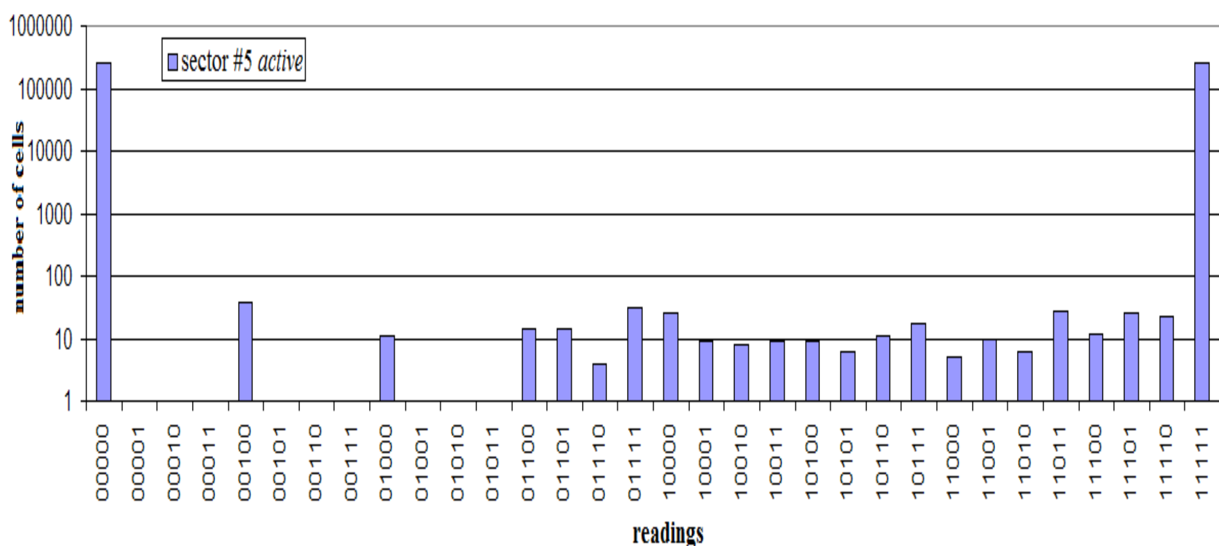

Fig.14 Bit-flip reading evolution distribution (from the first to the fifth reading) of the cells; each reading evolution shows the five logic values of a cell corresponding to each single reading

The same type of graph is used to represent the bit-flip evolution during all irradiation steps. In Fig. 15 this graph shows the bit-flip evolution stories, from the 113 krad to the 396 krad dose step (corresponding to a fluence increment of 10^9 ions/cm^{-2} for each step) for those sectors with the "0000" initial pattern (sectors 4, 8, 12, 16, 17), for both the *active* and

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passive case; each story type shows five logic values of a cell, corresponding to each single dose (i.e.: **010010** => $\mathbf{0}_{init.}$- $\mathbf{1}_{1}{}^{st}{}_{dose}$ - $\mathbf{0}_{2}{}^{nd}{}_{dose}$ - $\mathbf{0}_{3}{}^{rd}{}_{dose}$ -$\mathbf{1}_{4}{}^{th}{}_{dose}$ - $\mathbf{0}_{5}{}^{th}{}_{dose}$).

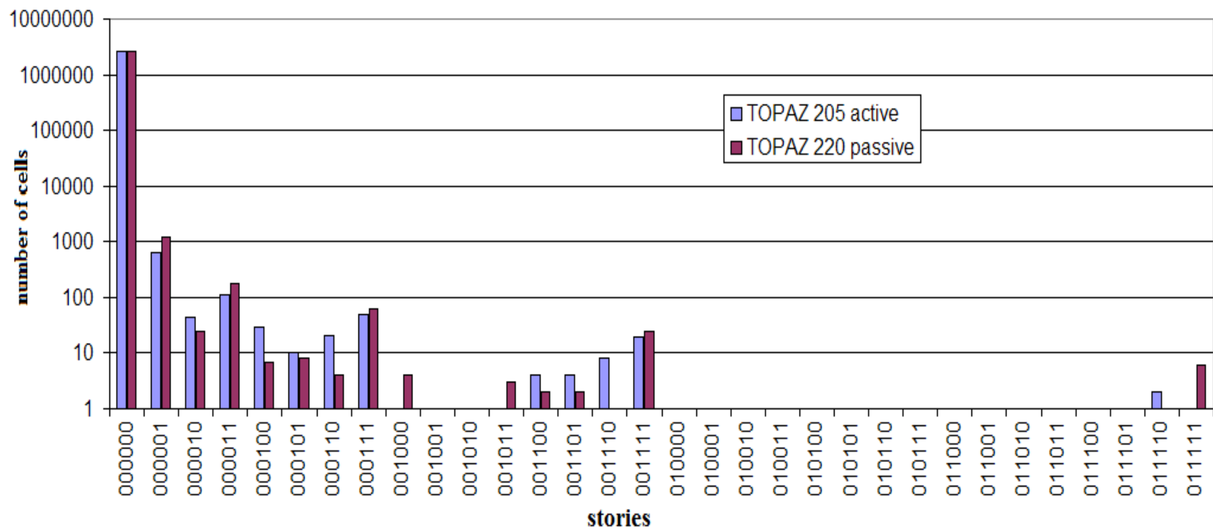

Fig.15 Bit-flip evolution stories distribution of the cells, from the 113 krad to the 396 krad dose step, for those sectors with the "0000" initial pattern; each story type shows five logic values of a cell, corresponding to each single dose.

It is possible to make some remarks about these results:

- Most cells, both in the *passive* and *active* case, maintain their initial state, during all the irradiation steps;
- Cells with just a single bit-flip are more than those ones with multiple bit-flips, both in the *passive* and *active* case;
- The memory in *passive* state (220) has more cells with a single bit-flip (i.e.: "000001", "000011", "000111", etc) than that one in *active* state (205);
- The memory in *active* state (205) has more cells with two bit-flips than that one in *passive* state (220);
- It is possible to note also that the stories with two bit-flips belong to those cells which change their state at higher doses. In the Table II this result is shown, even if going by small numbers;
- The cells with multiple bit-flips are not many, so it is not enough to make a remark.

TABLE II: STORIES WITH TWO BIT-FLIPS

	Memory 220	**Memory 205**
010000	0	1
011000	1	0
011100	0	0
011110	1	2
001000	4	1
001100	4	4
001110	1	8
000100	7	29
000110	4	21
000010	24	44

All these assumptions confirm what said before about the difference between the *active* and *passive* cases and the best response, at low doses, of the memory in *active* state. In addition, it is possible to deduce that the cells with multiple bit-flips could have the threshold voltage near the reading threshold voltage of the memory cell. In order to have more convincing results, from a statistical point of view, it would be necessary to analyze more data and so more memory chips. Using all these acquired data a *bit-flip tree* was created. This special tree allows to study in details the bit-flip evolution dose by dose, understanding how the bit-flips evolve. In Fig.16 it is shown this bit-flip tree for the *passive* case

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and for the sectors with "0000" as initial pattern. In this figure the first number shows the number of bit-flipped cells, the second one show the new logic state and the red number is the fluence (ions/cm2) of Boron ions. It is easy to see, dose by dose, the cells with a "0" to "1" bit-flip have an higher probability to stay in that logic state ("1") . In addition, if a cell does not change its logic state (remaining "0"), its probability to stay in that logic state ("0") decreases even if just a little.

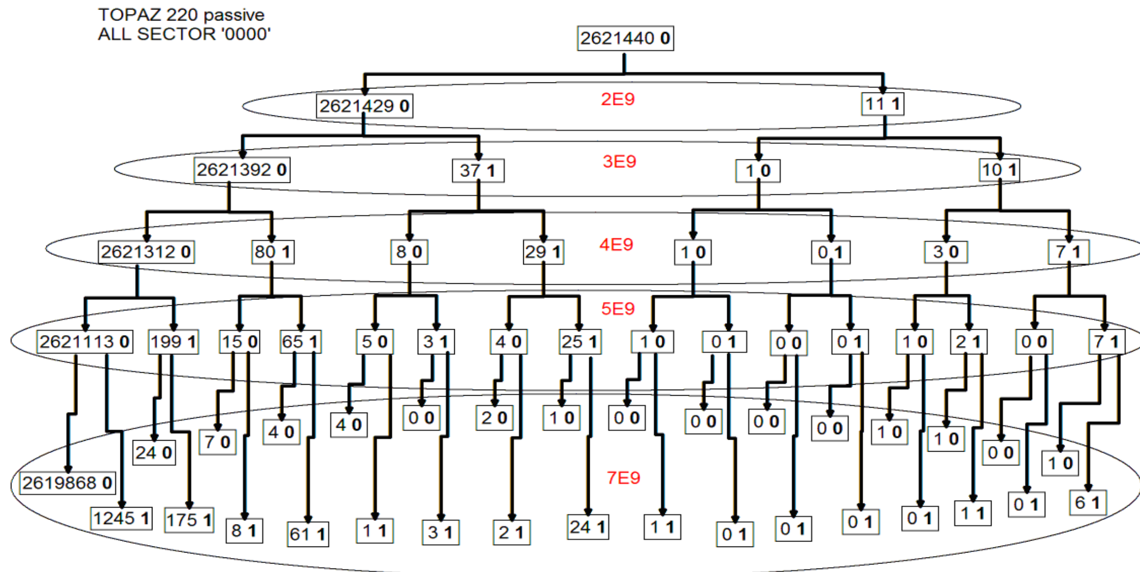

Fig.16 Bit-flip tree

VII. PREDICTIVE STATISTICAL MODEL OF THE MEAN THRESHOLD VOLTAGE SHIFT OF A MEMORY CELL

The main hypothesis which is put forward is that each particle hit induces a threshold voltage shift aliquot. At low doses, the shift value could be meanly low and negative, even if there could be a low probability to have positive voltage shifts. The "0" to "1" bit-flip is more probable. At high doses, it could be possible to have high and positive voltage shifts, justifying the possibility to have "1" to "0" bit-flips. In order to demonstrate that, all the data about the bit-flip stories were considered to create a predictive statistical model which can be used to estimate the mean threshold voltage shift of a single memory cell [29], [30]. The model was developed using the MatLab software.

First of all, as already said, the main consideration about this model is that each single particle (ion) induces a little threshold voltage shift when it goes through a memory cell. At this point, knowing the size of a cell (0.42um x 0.18um) and the ions fluence at each step, the mean number of ion hits per cell was calculated for each irradiation step as shown in the Table III.

TABLE III: MEAN NUMBER OF ION HITS PER CELL

STEP	FLUENCE (DOSE)	MEAN N° ION HITS PER CELL	MEAN CUMULATIVE ION HITS PER CELL
1	$2*10^9$ ions/cm^{-2} (113 krad)	1.512 (~1)	1.512 (~1)
2	$3*10^9$ ions/cm^{-2} (170 krad)	2.268 (~2)	3.780 (~3)
3	$4*10^9$ ions/cm^{-2} (226 krad)	3.024 (~3)	6.804 (~7)
4	$5*10^9$ ions/cm^{-2} (283 krad)	3.780 (~4)	10.584 (~10)
5	$7*10^9$ ions/cm^{-2} (396 krad)	5.292 (~5)	15.876 (~15)

A matrix with NxN cells was defined to store the memory cell threshold voltage (CTV). All the matrix cells were initialized with a threshold voltage on the basis of a Normal distribution (□ =6.65 V and □=0.15 for the programmed cells and □ =3.45 V and □=0.2 for the erased cells) thanks to the measures conducted with the MOSAID tester []. For

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each irradiation step a single memory cell could be hit N times by a particle, where N is the mean number of hits per memory cell. The algorithm chooses the coordinates (x, y) of the cells on the basis of a random distribution in order to guarantee the uniformity of irradiation. Hence, after each hit a memory cell will change its threshold voltage. The sign and the module of the shift was chosen on the basis of two different distributions: a Normal distribution for the sign (□ =-0.2V and □=0.15), in this way the probability of a negative shift is between the 90 and 98 % (low doses case); a Weibull distribution (A=0.0097 and B=0.5) for the module. After each step, a comparing was done between the updated threshold voltage of each memory cell and a threshold reading voltage (TRV) (from [] it is 5.2V); if the CTV is higher than TRV the memory cell value will zero otherwise one. So a new CTV distribution is created for each irradiation step. As study case, it was analyzed the sector 4 of the memory 220 (*passive* case) where the data pattern is "0000". After the statistical elaboration it is possible to compare the Experimental and the model bit-flip story tables. As visible in Fig. 17 and 18, there is a good fit between the two tables, without considering some mismatches due to the different initial conditions and approximations:

- for simplicity, the threshold voltage matrix was a square matrix of 524176 cells (724x724) instead of 524288 cells;
- the cells to be hit are chosen using a random distribution (to select row and column coordinates);
- one dose corresponds to an approximate (discrete) average number of ion hits on the basis of the area and the ion fluence calculation (1,2,3,4,5 hits/step);
- the threshold voltage of an hit cell is modified after every hit according two distributions: a normal distribution for the sign and a weibull distribution for the module of the threshold voltage.

'd_000000_d'	[523973]	000000	524095
'd_000001_d'	[117]	000001	130
'd_000010_d'	[1]	000010	8
'd_000011_d'	[58]	000011	22
'd_000100_d'	[1]	000100	5
'd_000101_d'	[0]	000101	2
'd_000110_d'	[0]	000110	4
'd_000111_d'	[15]	000111	10
'd_001000_d'	[0]	001000	0
'd_001001_d'	[0]	001001	0
'd_001010_d'	[0]	001010	0
'd_001011_d'	[0]	001011	0
'd_001100_d'	[0]	001100	0
'd_001101_d'	[0]	001101	0
'd_001110_d'	[0]	001110	1
'd_001111_d'	[11]	001111	4
'd_010000_d'	[0]	010000	0
'd_010001_d'	[0]	010001	0
'd_010010_d'	[0]	010010	0
'd_010011_d'	[0]	010011	0
'd_010100_d'	[0]	010100	0
'd_010101_d'	[0]	010101	0
'd_010110_d'	[0]	010110	0
'd_010111_d'	[0]	010111	0
'd_011000_d'	[0]	011000	0
'd_011001_d'	[0]	011001	0
'd_011010_d'	[0]	011010	0
'd_011011_d'	[0]	011011	0
'd_011100_d'	[0]	011100	0
'd_011101_d'	[0]	011101	0
'd_011110_d'	[0]	011110	0
'd_011111_d'	[0]	011111	0

Fig.17 Bit-flip story tables: statistical model (left), experimental (right)

In Fig.18 the cases with a single bit-flip are privileged also because of the low number of cells under test. In order to evaluate the orher cases (multi bit-flip) it is necessary to test more memory.

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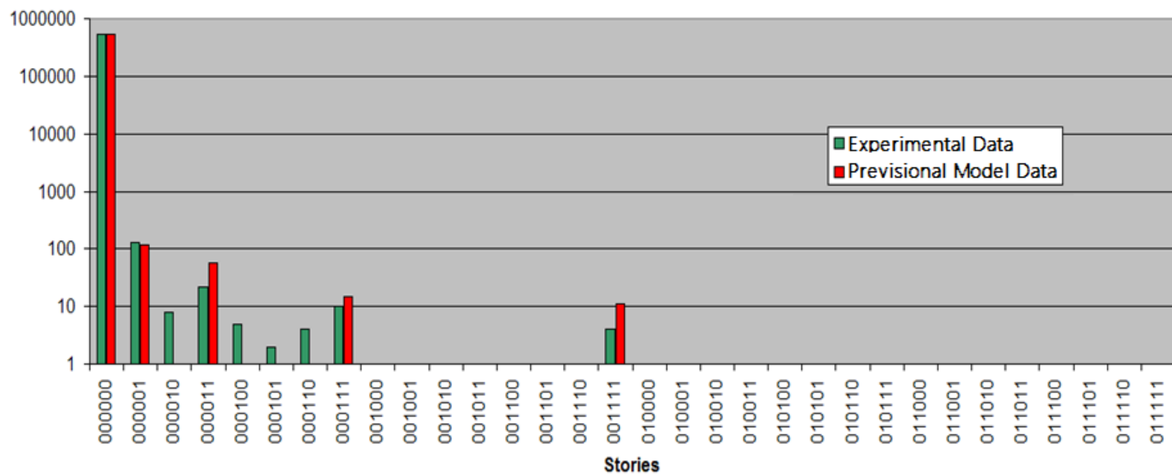

Fig.18 Bit-flip evolution stories distribution of the cells, comparing the experimental data and the statistical model data.

In Fig.19 there are the threshold voltage distributions of the memory cells of the sector 4 (memory 220), for each irradiation step. In Fig. 20 there is the actual threshold voltage distribution for the cells of the sector 4, acquired using the MOSAID tester device.

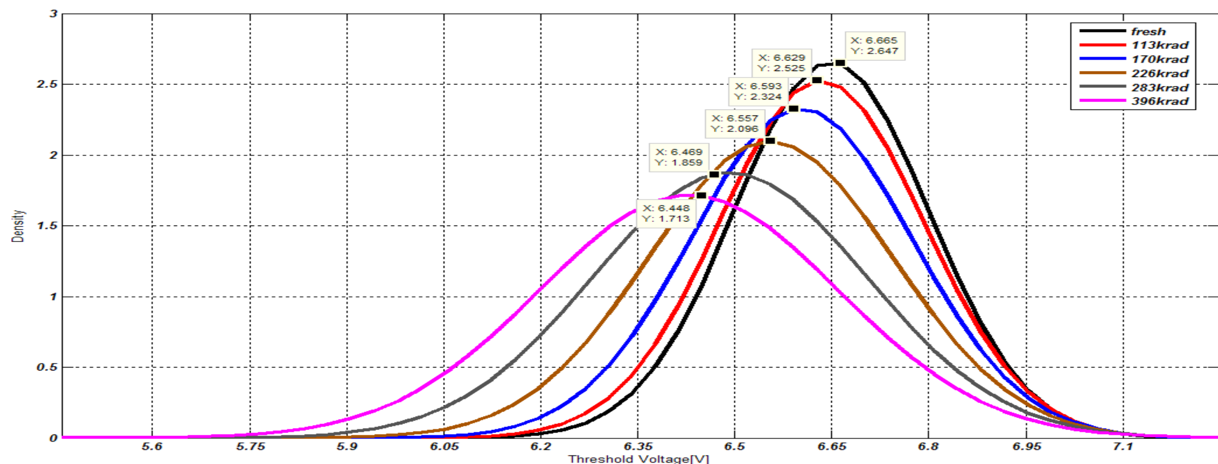

Fig.19 The threshold voltage distributions of the memory cells of the sector 4 (memory 220), for each irradiation step.

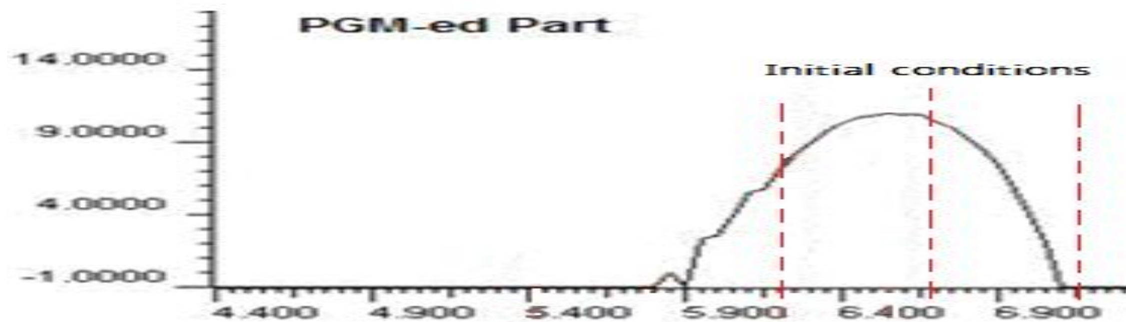

Fig.20 Actual threshold voltage distribution for the cells of the sector 4, acquired using the MOSAID tester device, the dotted red lines show the initial condition of the distribution before the irradiation

Comparing the two figures it is possible to see how much the model is good. For example, the mean threshold voltage shift for the actual distribution is about 200 mV while for the statistical distribution is about 230 mV.

Using this it is possible to confirm that each particle hit induces a threshold voltage shift. At low doses, the shift value will be meanly low and negative, even if there is a low probability to have positive voltage shifts. The "0" to "1" bit-flip is more probable. At high doses, it is possible to have high and positive voltage shifts, justifying the possibility to have "1" to "0" bit-flips.

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VIII. CONCLUSION

It is possible to summarize all the key points of this work, presented in this paper. This work concerned the study and test of the ELT transistors (radiation-hard "by layout" devices) in "fresh" state (before the irradiation test) and the analysis of the TOPAZ memories irradiated with Boron ions up to 1.4 Mrad to test their radiation-tolerance TID (Total Ionizing Dose). As regards the ELT transistors: all the electrical features of these transistors and the differences between the drain-in and drain-out case were confirmed; there are not considerable differences between the three ELT types (with one, two and four gate sides contacted), so it is possible to use that one with a single gate side contacted, in order to save area.

Concerning the TOPAZ memories: it is possible to affirm that the TOPAZ memories can be considered working properly up to a dose of about 400 krad; over this dose there will be many irreversible failures in several sectors, confirmed by the impossibility to program the sectors again; an higher radiation-hardness was seen when the memory was irradiated in *active* case, because of the electrical field which eases the recombination of the trapped charges. Some statistical data elaborations were conducted in order to understand the trend of the bit-flip of the cells with the dose. Using these data a predictive model was defined to estimate the mean variation of the memory cell threshold voltage shift with the dose.

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